

What is claimed is:

1 1. A circuit board comprising:
2 a first reference plane layer;
3 a second reference plane layer;
4 a dielectric layer between the first and second reference plane layers; and
5 a resistive element between the first and second reference plane layers.

1 2. The circuit board of claim 1, wherein the resistive element is a resistive
2 layer formed of a resistive material; the resistive layer between the dielectric layer and
3 the first reference plane layer.

1 3. The circuit board of claim 2, further comprising a second resistive layer
2 between the dielectric layer and the second reference plane layer.

1 4. The circuit board of claim 2, wherein the resistive layer extends
2 substantially across and is in contact with a surface of the first reference plane layer.

1 5. The circuit board of claim 2, further comprising a decoupling capacitor
2 having first and second electrodes, the first electrode electrically contacted to the resistive
3 layer and the second electrode electrically contacted to the second reference plane layer.

1 6. The circuit board of claim 5, wherein the decoupling capacitor is between
2 the first and second reference plane layers.

1 7. The circuit board of claim 5, wherein the decoupling capacitor comprises a
2 surface mount technology (SMT) capacitor embedded between the first and second
3 reference plane layers.

1 8. The circuit board of claim 5, wherein the decoupling capacitor has a first
2 dimension and a second dimension less than the first dimension, the decoupling capacitor

3 positioned such that its second dimension determines spacing between the first and
4 second reference plane layers.

1 9. The circuit board of claim 8, wherein the decoupling capacitor is placed
2 on its side.

1 10. The circuit board of claim 5, wherein the decoupling capacitor has a
2 vertical dimension and a horizontal dimension, the decoupling capacitor positioned such
3 that its vertical dimension determines spacing between the first and second reference
4 plane layers.

1 11. The circuit board of claim 5, wherein the decoupling capacitor has a first
2 side and a second side, the first and second sides being generally parallel to each other,
3 the first and second electrodes arranged at the first and second sides, and the decoupling
4 capacitor positioned such that the first and second sides are generally perpendicular to
5 main surfaces of the reference plane layers.

1 12. The circuit board of claim 11, further comprising:
2 a first insulator between a first side surface of the first electrode and the
3 resistive layer, wherein a second side surface of the first electrode is electrically
4 connected to the second reference plane layer; and
5 a second insulator between a first side surface of the second electrode and
6 the second reference plane layer, wherein a second side surface of the second electrode is
7 electrically connected to the resistive layer.

1 13. The circuit board of claim 2, further comprising plural decoupling
2 capacitors between the resistive layer and the second reference plane layer.

1 14. The circuit board of claim 13, further comprising a second resistive layer
2 between the plural decoupling capacitors and the second reference plane layer.

1 15. The circuit board of claim 1, wherein the resistive element comprises a
2 discrete resistor having one end electrically connected to the first reference plane layer,
3 the circuit board further comprising a decoupling capacitor having first and second
4 electrodes, the first electrode electrically connected to another end of the discrete resistor,
5 and the second electrode electrically connected to the second reference plane layer.

1 16. The circuit board of claim 1, further comprising a core including the first
2 reference plane layer, second reference plane layer, dielectric layer, and resistive element.

1 17. The circuit board of claim 16, further comprising signal layers on at least
2 one side of the core.

1 18. The circuit board of claim 1, further comprising a plurality of decoupling
2 capacitors between the first and second reference plane layers, wherein the dielectric
3 layer comprises a template having plural holes to receive the decoupling capacitors.

1 19. A system comprising:
2 an integrated circuit device; and
3 a circuit board on which the integrated circuit device is mounted, the
4 circuit board comprising:
5 a first reference plane layer;
6 a second reference plane layer;
7 a dielectric layer between the first and second reference plane
8 layers; and
9 a resistive element between the first and second reference plane
10 layers.

1 20. The system of claim 19, wherein a resistive element is a resistive layer
2 formed of a resistive material, the resistive layer between the dielectric layer and the first
3 reference plane layer.

1 21. The system of claim 20, further comprising a second resistive layer
2 between the dielectric layer and the second reference plane layer.

1 22. The system of claim 20, further comprising a decoupling capacitor having
2 first and second electrodes, the first electrode electrically connected to the resistive layer
3 and the second electrode electrically connected to the second reference plane layer.

1 23. The system of claim 22, wherein the decoupling capacitor is between the
2 first and second reference plane layers.

1 24. The system of claim 20, further comprising plural decoupling capacitors
2 between the resistive layer and the second reference plane layer.

1 25. The circuit board of claim 19, wherein the resistive element comprises a
2 discrete resistor having one end electrically connected to the first reference plane layer,
3 the circuit board further comprising a decoupling capacitor having first and second
4 electrodes, the first electrode electrically connected to another end the discrete resistor,
5 and the second electrode electrically connected to the second reference plane layer.

1 26. A method of making a circuit board, comprising:
2 forming first and second reference plane layers;
3 forming a dielectric layer between the first and second reference plane
4 layers; and
5 forming a resistive element between the first and second reference plane
6 layers.

1 27. The method of claim 26, wherein forming the resistive element comprises
2 forming a resistive layer between the dielectric layer and the first reference plane layer.

1 28. The method of claim 27, further comprising forming a second resistive
2 layer between the dielectric layer and the second reference plane layer.

1 29. The method of claim 26, further comprising forming a core that includes
2 the first and second reference plane layers, the dielectric layer, and the resistive element.

1 30. The method of claim 29, further comprising forming signal layers on
2 either side of the core.

1 31. The method of claim 30, further comprising forming another core having
2 first and second reference plane layers, the dielectric layer, and the resistive element.

1 32. The method of claim 26, wherein forming the dielectric layer comprises
2 providing a template having a plurality of holes onto the second reference plane layer.

1 33. The method of claim 32, further comprising providing a plurality of
2 decoupling capacitors into the holes of the template.

1 34. The method of claim 33, further comprising attaching the first reference
2 plane layer to another side of the template.

1 35. The method of claim 26, further comprising providing a plurality of
2 decoupling capacitors between the first and second reference plane layers.

1 36. The method of claim 35, wherein providing the decoupling capacitors
2 comprises providing surface mount technology (SMT) decoupling capacitors.

1 37. A circuit board comprising:
2 a first reference plane layer;
3 a second reference plane layer; and
4 a decoupling capacitor between the first and second reference plane layers,
5 the decoupling capacitor having a first side and a second side generally parallel to the
6 first side, the decoupling capacitor further having a first electrode at the first side and a
7 second electrode at the second side, the decoupling capacitor being placed on its side

8 such that first and second sides of the decoupling capacitor are generally perpendicular to
9 the main surfaces of the first and second reference plane layers.